QUARTERLY REPORT NO. 12

FOR

ANALOG-TO-DIGITAL CONVERTER

CONTRACT NO. N00014-87-C-0314

1 January 1991—31 March 1991

ARPA Order Number:	9117
Program Code Number:	7220
Amount of Contract:	$3,152,507
Name of Contractor:	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655936, M.S. 105 Dallas, Texas 75265
Effective Date of Contract:	30 March 1987
Contract Expiration Date:	31 July 1991
Contract Number:	N00014-87-C-0314
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Short Title of Work:	GaAs A-to-D Converter
Contract Period Covered by Report:	1 January 1991—31 March 1991

16 April 1991

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I. SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high-sampling-rate analog-to-digital converter (ADC) and a high-resolution GaAs ADC.

B. ADC Program Overview

A p-channel JFET (PJFET) SPICE model and design have been delivered to Hughes for the 12-bit ADC design. A new lot of material has been started using essentially the same PJFET design to ensure that the SPICE model parameters can be duplicated.

We have continued to make progress in the design and layout of the 12-bit ADC. The input sample-and-hold circuits, have been converted from n-channel JFETs to p-channel JFETs, to be compatible with our process changes.

A proposal has been submitted to a classified government program to continue and enhance the efforts started under this DARPA program to complete the 5-bit and 8-bit ADCs. The 12-bit ADC will continue to be the main thrust of our on-going DARPA program.

II. PROGRESS REPORT

A. Process Development

TI has supplied a new SPICE model and design for the PJFET to Hughes to incorporate in the 12-bit ADC design. A modification to our original PJFET process was needed to increase the gate-drain breakdown voltage. This process change has been incorporated in the PJFET lot currently being processed to ensure that SPICE parameters and breakdown voltages given to Hughes can be duplicated in the laboratory. This lot focused only on the PJFETs and eliminated all unnecessary process steps required for the HBTs, resistors, capacitors, and multilevel metal to minimize cycle time. A second lot has been started in the GaAs pilot line using this same process. Preliminary results of in-process probing of the first lot run in CRL suggests that the new process will meet the required breakdown voltage requirements. During the coming month both lots should be completed and wafer probed to fully characterize the PJFETs.

B. ADC Process Transfer

Current-induced degradation of I-V characteristics in AlGaAs/GaAs HBTs has been reported by TRW and NTT for mesa HBTs with beryllium-doped base. Similar degradation has been obtained by TI for their microwave zinc-doped mesa HBTs. Because of these results, TI has undertaken (with IR&D funding) a study of potential degradation of ADC overgrowth HBTs. HBTs from our most recent pilot-line lot (Lot 104), which exhibited the 45 percent yield wafer, were packaged and placed on stress test. To accelerate the potential degradation process, our standard $5 \times 5\ \mu m^2$ emitter HBT was operated at 6 mA, which is 6× the maximum design current used in both the 5-bit ADC and the 12-bit ADC. After approximately 1000 hours at 250°C ambient, the collector currents shows less than 15 percent change; this is significantly better than reported results in the open literature. In addition, no decrease in dc current gain resulting from an increase in the base current after stress has been detected. Figure 1 shows the HBT Gummel plot after 250°C bias-temperature stress. It can be seen that for the low voltage range, the base current is below the detection level and current gain is greater than 1000 at the 1-mA operating current.

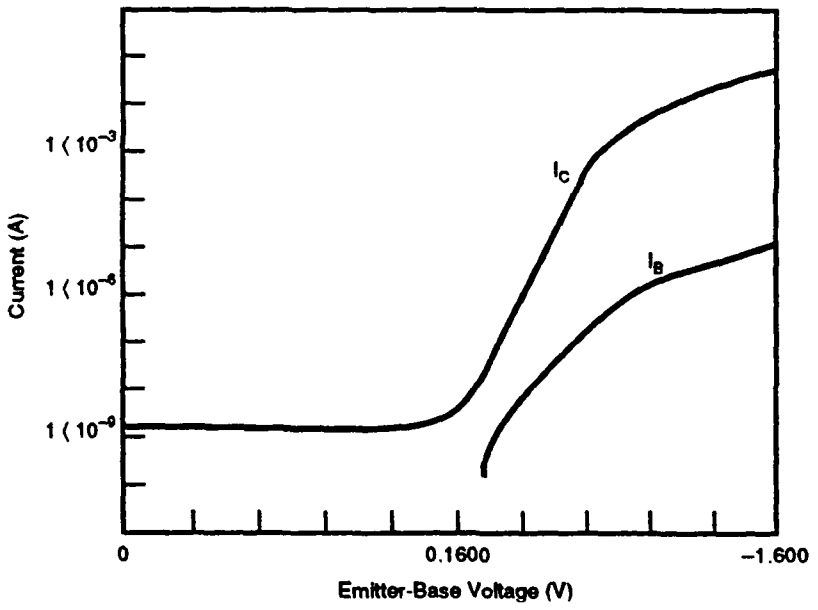

Figure 1. HBT Gummel plot after 1000 hours, 250°C bias-temperature stress.

C. Circuit Design/Testing

Hughes continues to make progress in the design and layout capture of the 12-bit ADC. Device layouts for the p-channel JFET, 5 × 5-μm HBT, Schottky diode, and zener diode were provided by TI early in the quarter and subsequently added to the layout database. The input sample-and-hold circuit, which consists of differential input buffers, sampling gates, and hold amplifiers has been converted from n-channel to p-channel JFET devices. A novel current mirror circuit using depletion-mode p-channel JFETs has been employed as high-impedance active load for the high-resolution amplifiers. The current mirror circuit reduces circuit sensitivity to JFET threshold voltage and transconductance process variations. The circuit approach should increase the yield of functional 12-bit ADCs.

In addition, an improved 8-bit digital-to-analog converter (DAC) circuit has been designed. The 8-bit DAC is a sub-element of the 12-bit ADC (Figure 2) that provides a precision output current that is subtracted from the sampled analog input signal to form a residue signal. The residue signal is amplified and quantized by the 5-bit ADC circuit to form the final 12-bit word. The 8-bit DAC output current transfer function must be linear to 0.006 percent to ensure overall ADC accuracy. Wafer-level testing of the 8-bit DAC sub-element contained on the 12-bit ADC building block mask set indicated the required linearity requirement would not be met. The accuracy limitations of the DAC, because of process variations, were investigated and subsequently understood. In response, a novel 8-bit DAC circuit topology was developed that significantly improved the circuit's sensitivity to process variations, while providing external trim capability to ensure that the 0.006 percent accuracy requirement can be met.

A new model revision and device layout for the p-channel JFET was provided by TI in February. A comparison between the Revision 0 and Revision 1 p-channel JFET device characteristics is shown in Table 1. Key parameters driving the performance of the 12-bit ADC are highlighted. Of primary importance are the PJFETs output impedance and gate-to-drain parasitic capacitance, since these devices are used as active loads for high-resolution amplifiers within the 12-bit ADC.

The new model reflects a significant reduction in gate-to-drain capacitance (C_{gd}), which will improve the maximum conversion rate of the 12-bit ADC. It is interesting to note that this capacitance is nearly identical to the parasitic capacitance projected for the original n-channel JFET design. Output conductance of the updated model shows a reduction from 50 kΩ to 20 kΩ, which will reduce the linearity of the high-resolution amplifiers by roughly 1-bit. The impact on the 12-bit ADC will be an overall reduction in integral linearity. Improvements in this parameter by TI will result in direct improvements in the 12-bit ADC accuracy without circuit design or layout modifications.

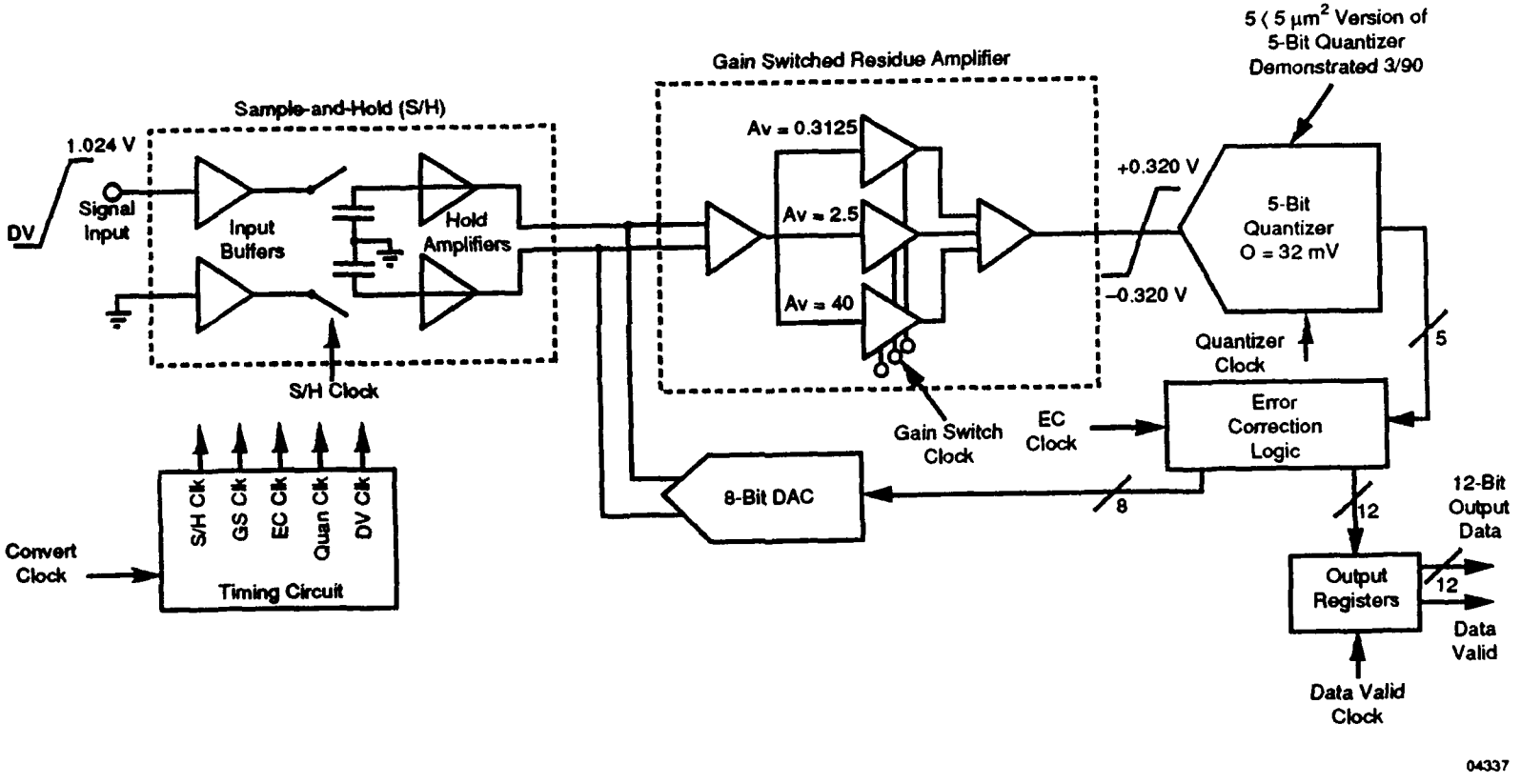

Figure 2. 12-bit analog-to-digital converter block diagram.

Table 1. Comparison of old versus new p-channel JFET Characteristics for 12-bit ADC

Parameters	Revision 0 Model (old)	Revision 1 Model (new)
Minimum gate length	1.5 μm	2.0 μm
Width for 1-mA I_{ds} sat	45 μm	45 μm
V_{ds} minimum	2 V	4 V
C_{gd}	126 ff	27 ff
Output conductance	50 kΩ	20 kΩ

Finally, the minimum required drain-to-source voltage (V_{ds}) for operation in the saturation region has increased from 2 V to 4 V. This shift directly reduces the available voltage compliance range within each amplifier design by approximately 4 V, since two PFET devices are used in cascode to maximize the total output conductance. As a result, tighter control of the PFETs pinch-off voltage will be required for proper circuit operation. The PFET model and device layout change by TI required the design and layout of each amplifier to be reviewed and modified by Hughes to ensure proper circuit operation. This effort was not anticipated, and will delay mask set release until June 1991.

Layout of the timing and control circuitry for the 12-bit ADC is approximately 90 percent complete, the sample-and-hold is approximately 90 percent complete, the 5-bit quantizing element is 80 percent complete, and the error-correction circuitry is 25 percent complete. Circuit design changes to all the circuits affected by the PFET model revision update are approximately 90 percent complete.

D. New ADC Proposal

The TI/Hughes team has submitted a new proposal (10 April 1991) to a classified government program to complete and enhance the 5-bit and 8-bit ADC work started under this DARPA program. The proposal offers a two-pass design cycle for the 8-bit ADC. In the first-pass design, sample-and-hold circuits would be added to both 5-bit and 8-bit ADCs. In addition, both ADCs would have ECL-compatible output levels. All designs in the first-pass design would be made with an improved 5 × 5-μm^2 emitter HBT. After completing the first-pass design, fabrication, and characterization, a second-pass design of the 8-bit-only ADC would be made using a scaled HBT with 2 × 5-μm^2 emitters to improve the dynamic range to 7 bits for a 500-MHz bandwidth signal.

III. PERSONNEL ASSIGNMENTS

There have been no changes in personnel.

IV. PLANS FOR NEXT QUARTER

- Hughes:
  - Complete 12-bit ADC layout and release database for processing
- TI:
  - CRL will continue interfacing with Pilot Line to ensure smooth process transfer
  - Pilot Line will continue processing lots in progress
  - Pilot Line will start processing 12-bit ADC

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